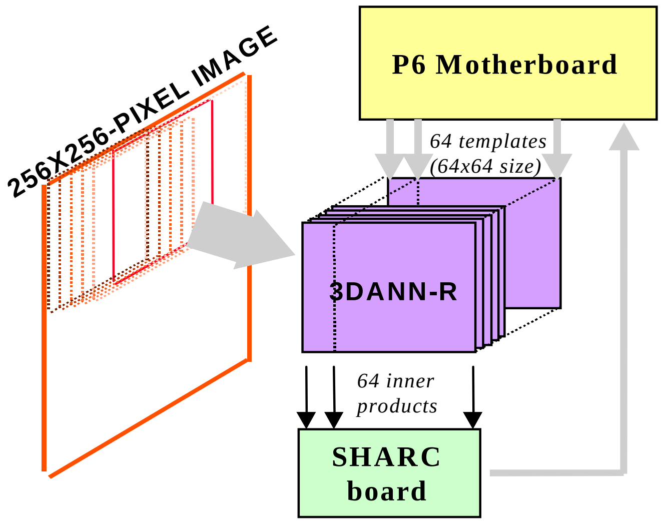
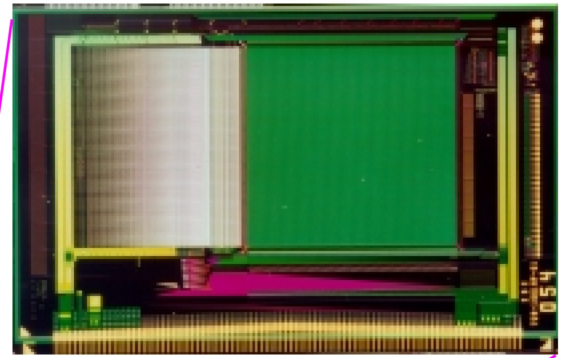
VIGILANTE develops a new architecture for intelligent vision systems and demonstrates functional sugar-cube-sized tera-ops processor for ATR

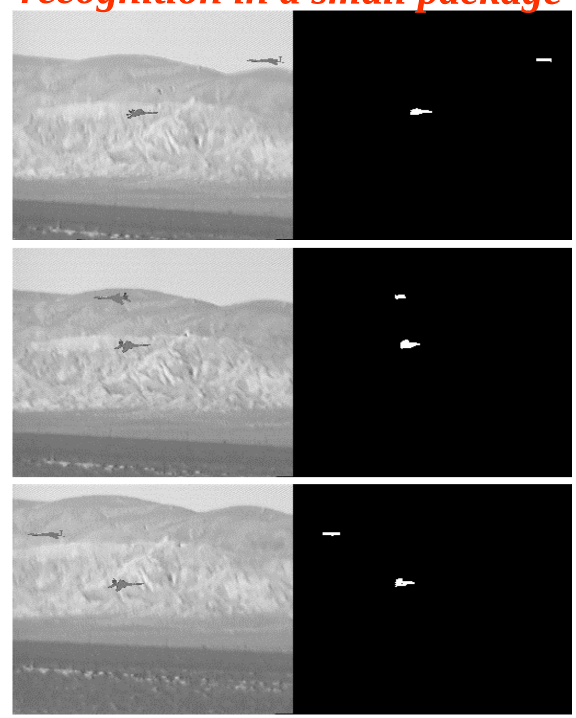
VIGILANTE Processing Architecture

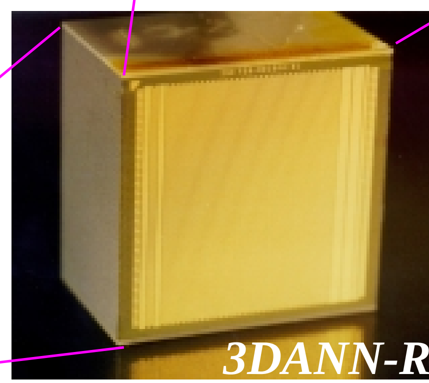




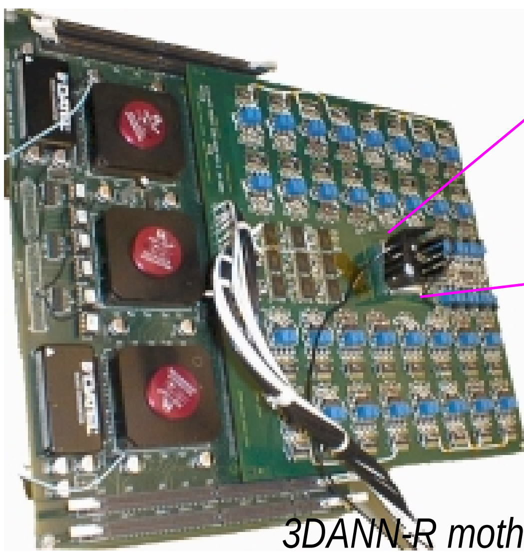
3DANN-R mixed-signal ASIC using 0.6 µm CMOS and over 1 million transistors

Achieving unprecedented real-time automatic target recognition in a small package





3D Convolution processor, containing 64 row convolver IC's capable of 1 TeraOPS in a 1.4cm x 1.45cm x .75 cm/5W package



3DANN-R motherboard/daughterboard providing A/D, memory, and interface to host computer

What is the 3DANN?

Massively parallel analog processor

– Computes 64--4096 element inner products in 250 nsec

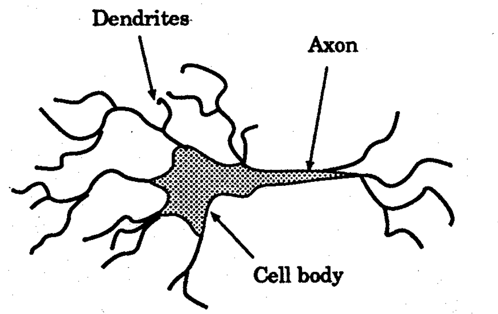
– Holds 64, digitally loaded, inner product templates (load time 1 msec)

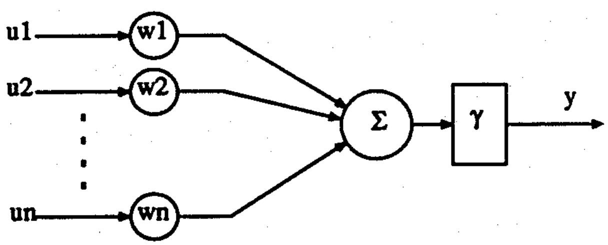
– Shifts in 64 data elements every 250 nsec

– Capable of fully evaluating a 256x256 2-D sensor image in 16 msec using 64 (64x64) kernels (loaded as inner product templates)

– Processor size 1.5 cm^3 consuming 5watts power

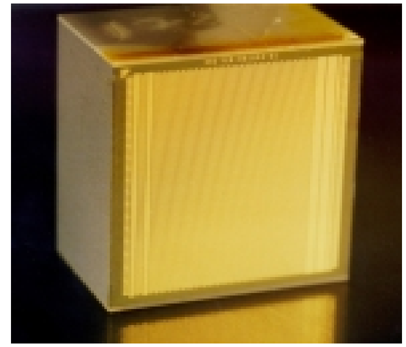
How Does the 3DANN Work?





Functional representation of a neuron

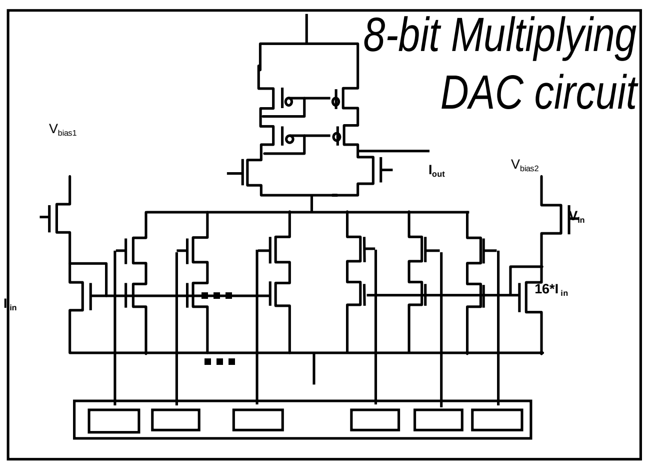
3DANN
64 Stacked Slices
1.5 cc / 5 W



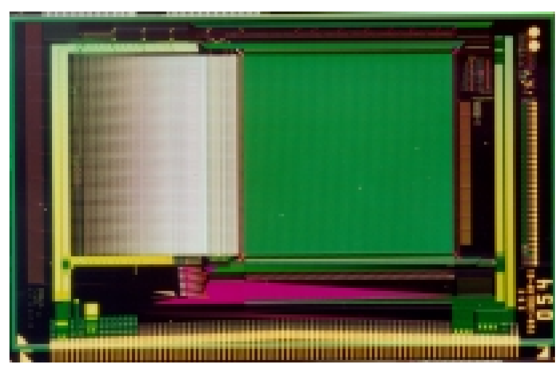
Ultrafast Inner-Product/Convolution Engine

ASIC Slice
64 channels

Shifts on a single data element each clock, stores 64 data elements and 64, 64 element template data for evaluation
Evaluates (multiply/sum) data and template every 250 nsec

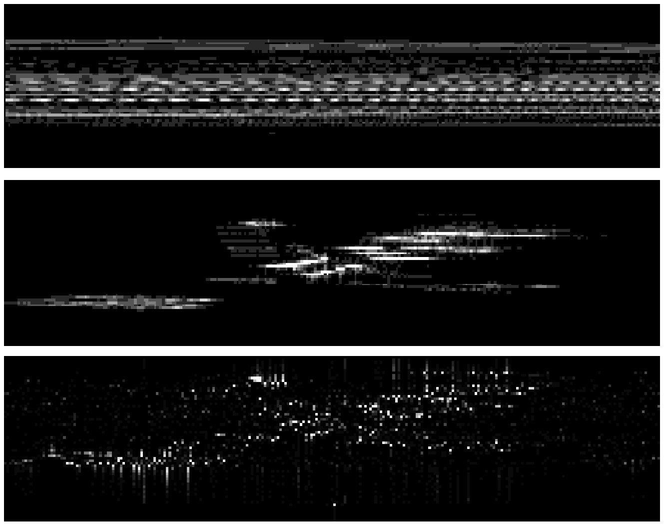


8-bit Multiplying DAC circuit



Uses of 3DANN

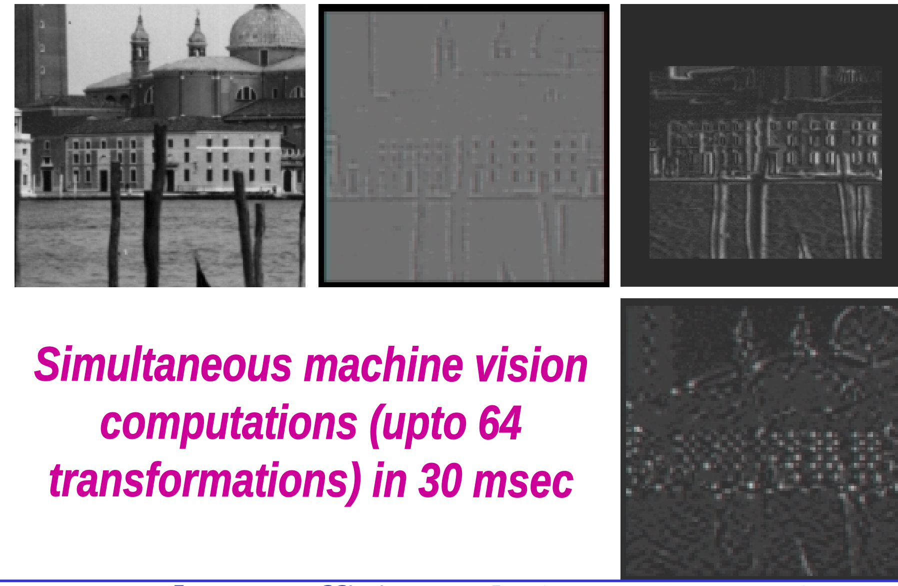
SAR data processing in 1 msec



Raw data (64x256)

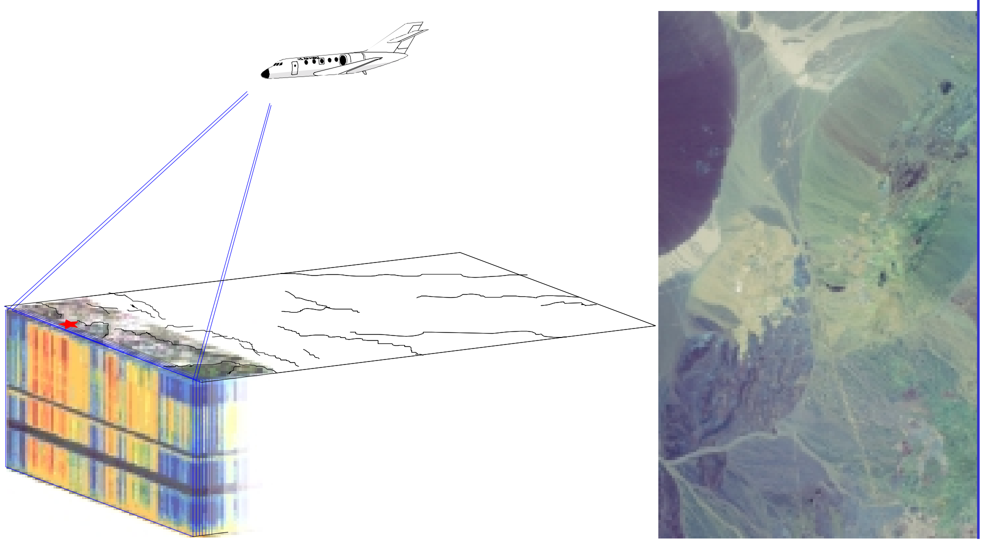
Processed data using FFT (~30msec on a 100MHz DSP)

Uncorrected 3DANN-R outputs

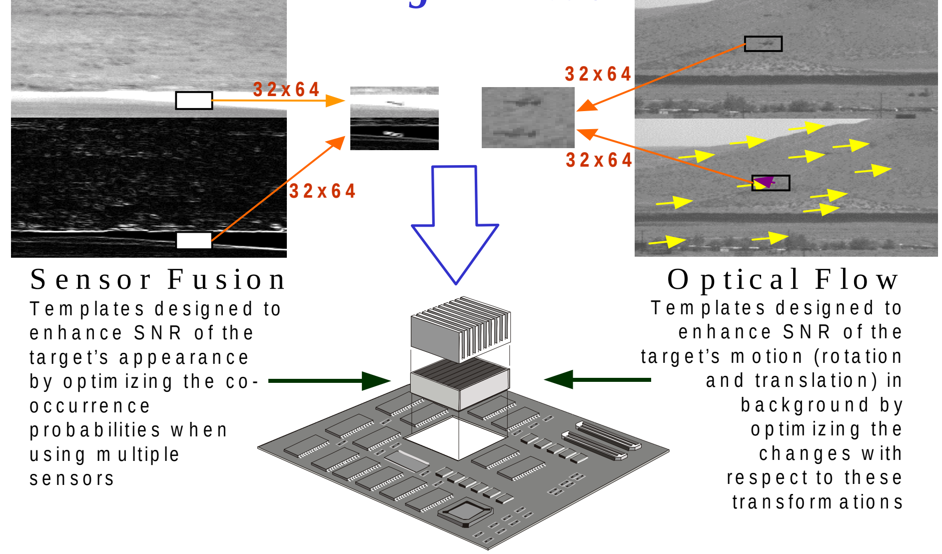


Simultaneous machine vision computations (upto 64 transformations) in 30 msec

Processing of hyperspectral data cube



Faster and more efficient solutions to sensor fusion and target detection



Target Recognition
Using the VIGILANTE Cube

- Problem

  Locate a known target (cruise missile) in a sensor image

- Difficulties

  Viewing geometry

  Lighting

  Background conditions

  Target scale

- Approach

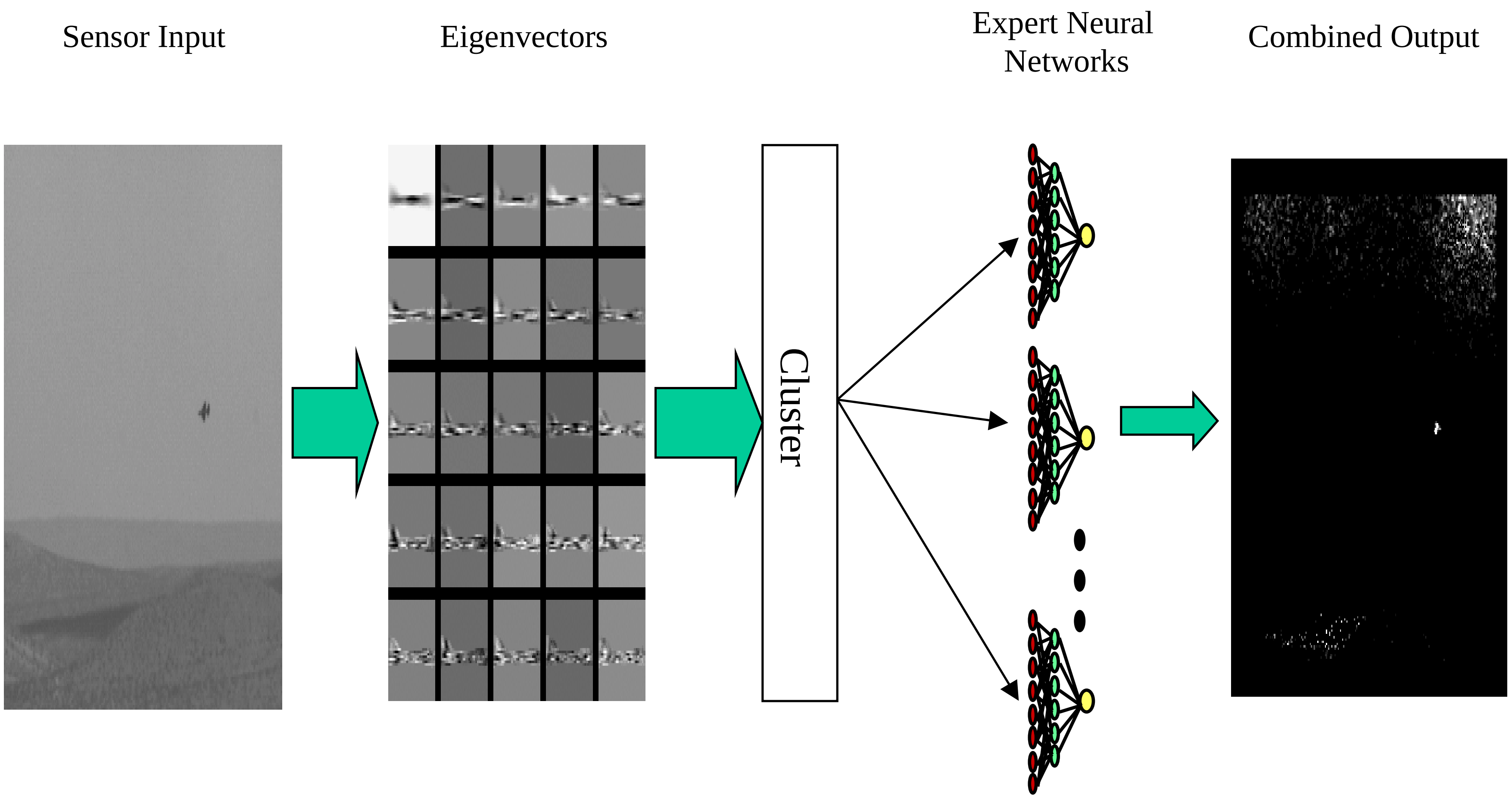
  Develop filters that account for changes in view, scale and lighting, separating out background from target

  Convolve image with filters (resulting in n descriptors for each sub-window)

  Associate each descriptor to a known group (segment)

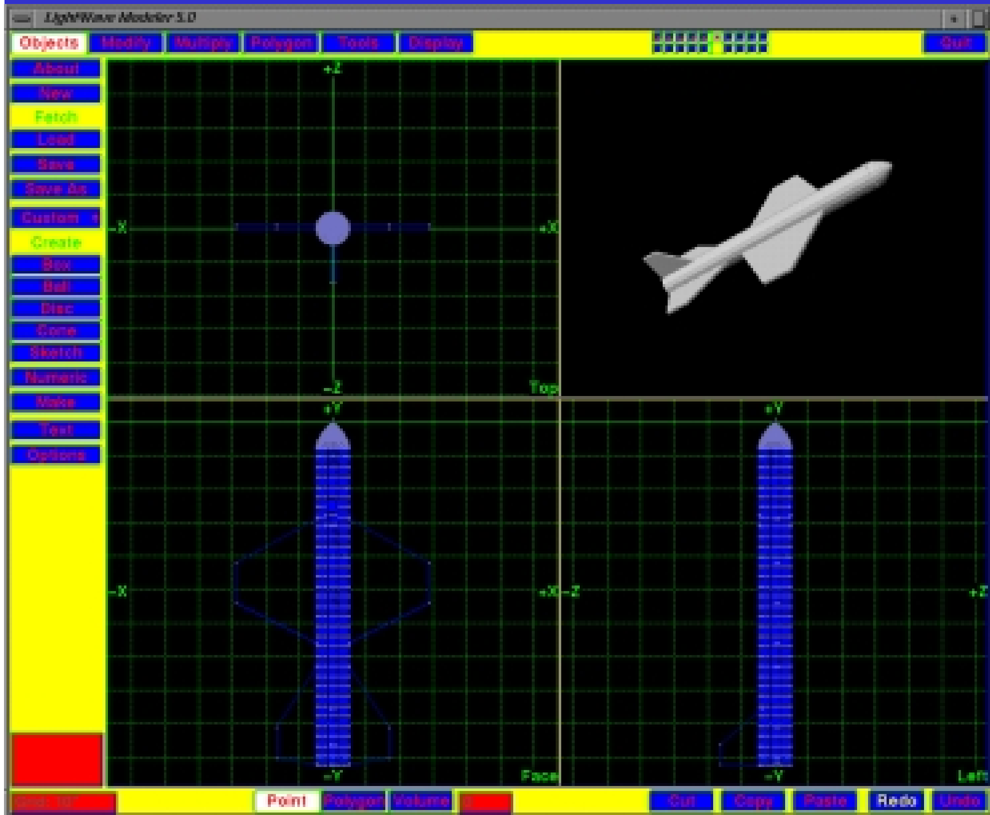
  Classify each descriptor as to target/non-target with expert on that particular segment

Target recognition methodology



Using neural network classifiers on Eigenvector projections to recognize/identify targets of various lighting conditions, scales and orientations.

Generating Templates



Generate Images from 3D Model by specifying:

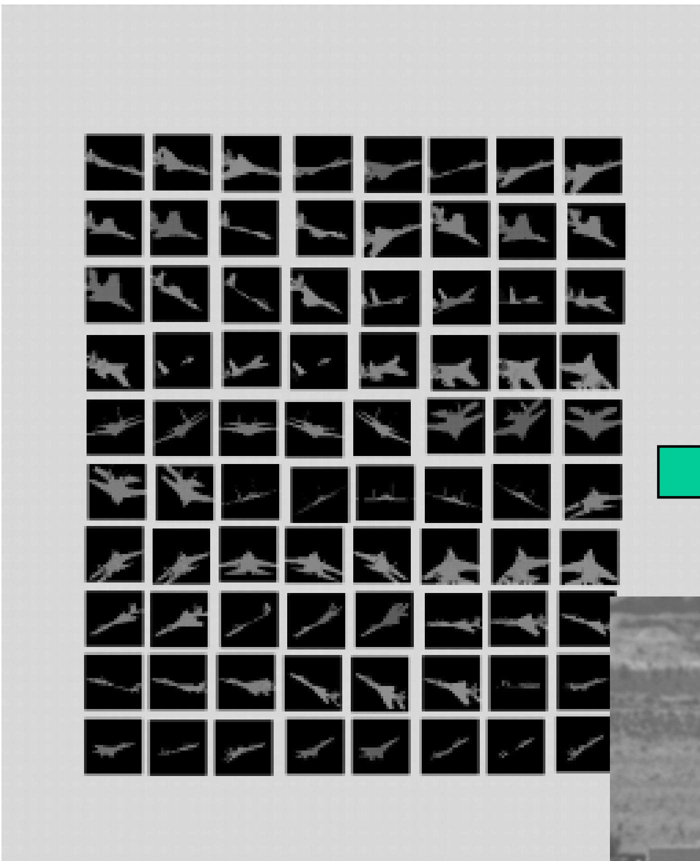
- Orientation
- Scale
- Frame Size
- Sampling Rate
- Camera/Lighting Information

Build Textured 3D Model from:

- Model Specifications
- Digital Images
- Camera Specifications and Locations
- Key Reference Points and Axes

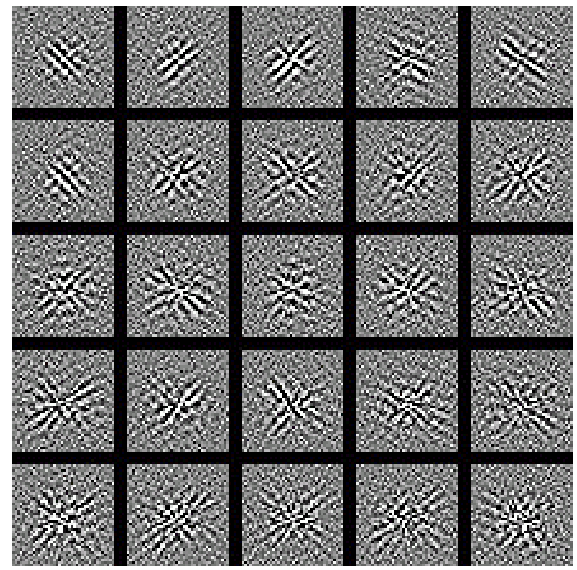
Generating Templates

Synthetic Targets

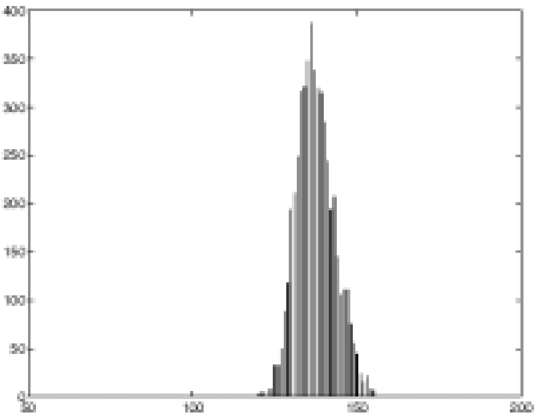


Embedded in Background

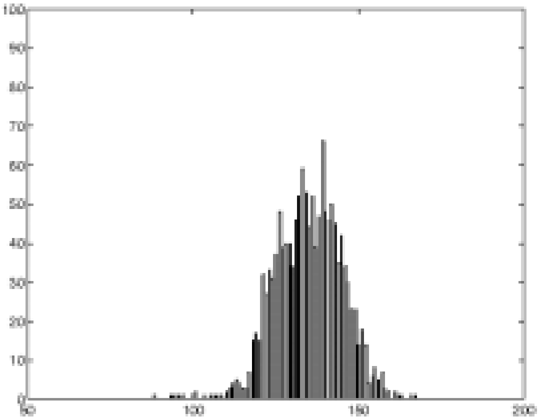
Filters Optimally Separate Targets in Background From Background (DPCA)



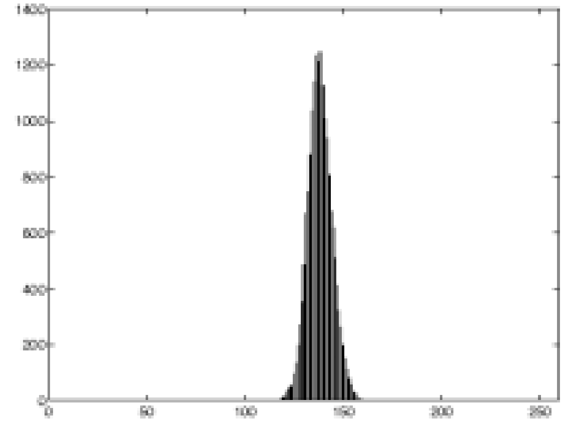
Using Filters on the 3DANN



Filter 0

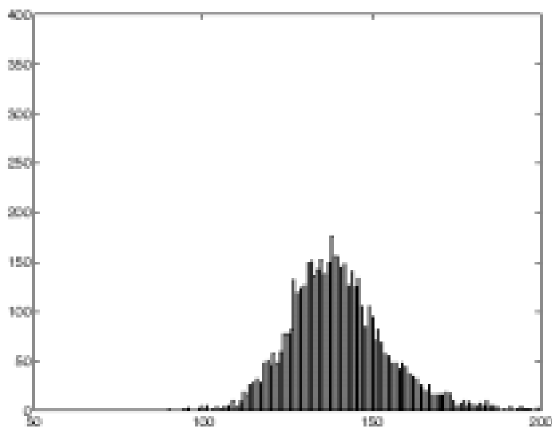


Filter 1

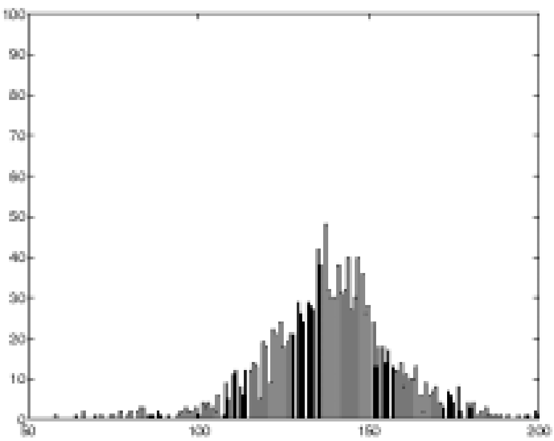


Filter 2

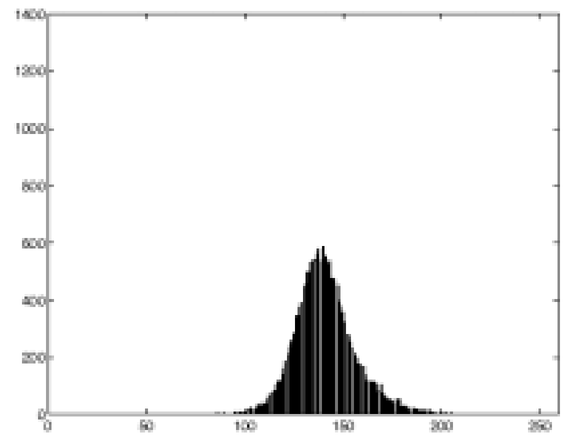
Background Sub-Window Outputs



Filter 0



Filter 1

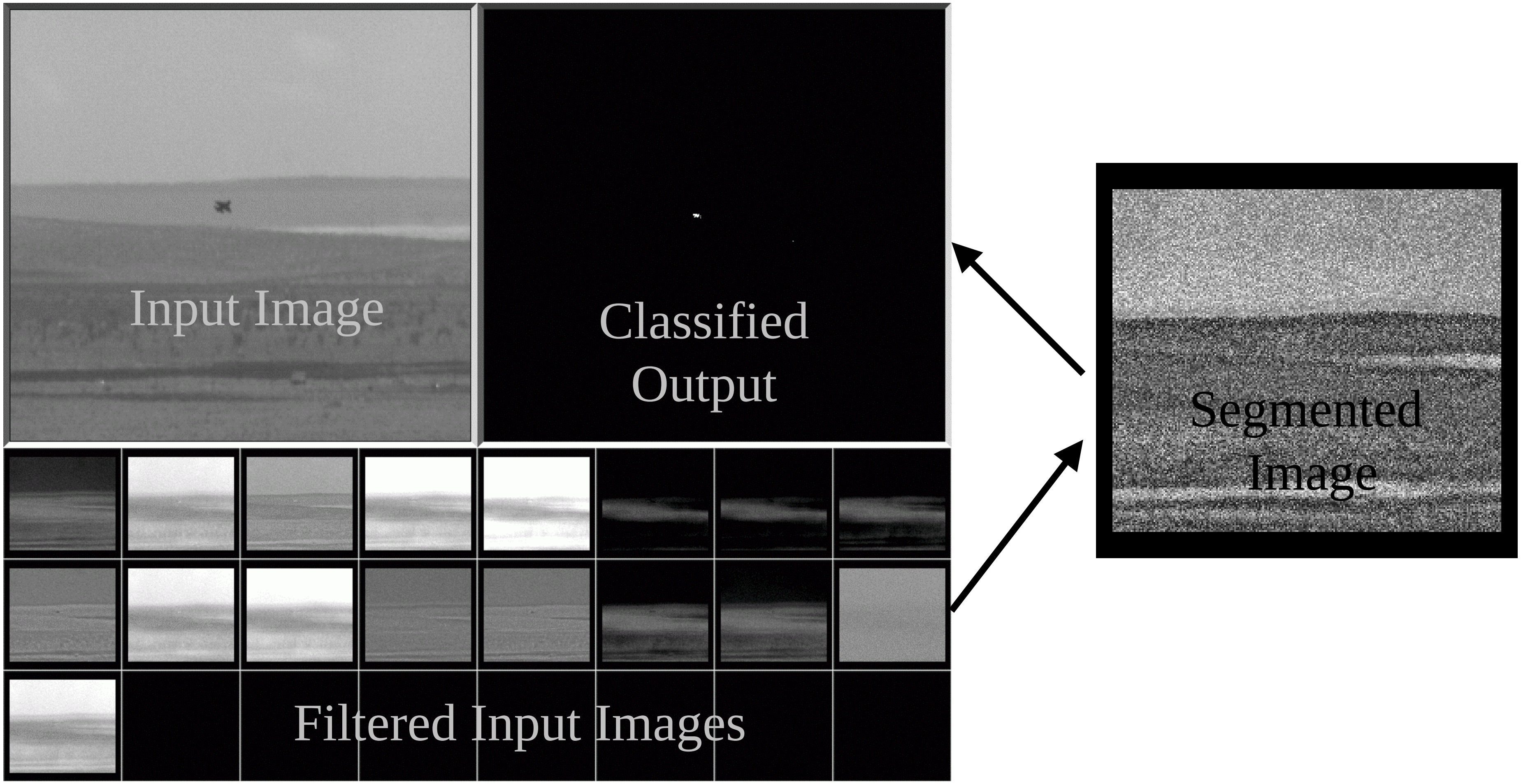


Filter 2

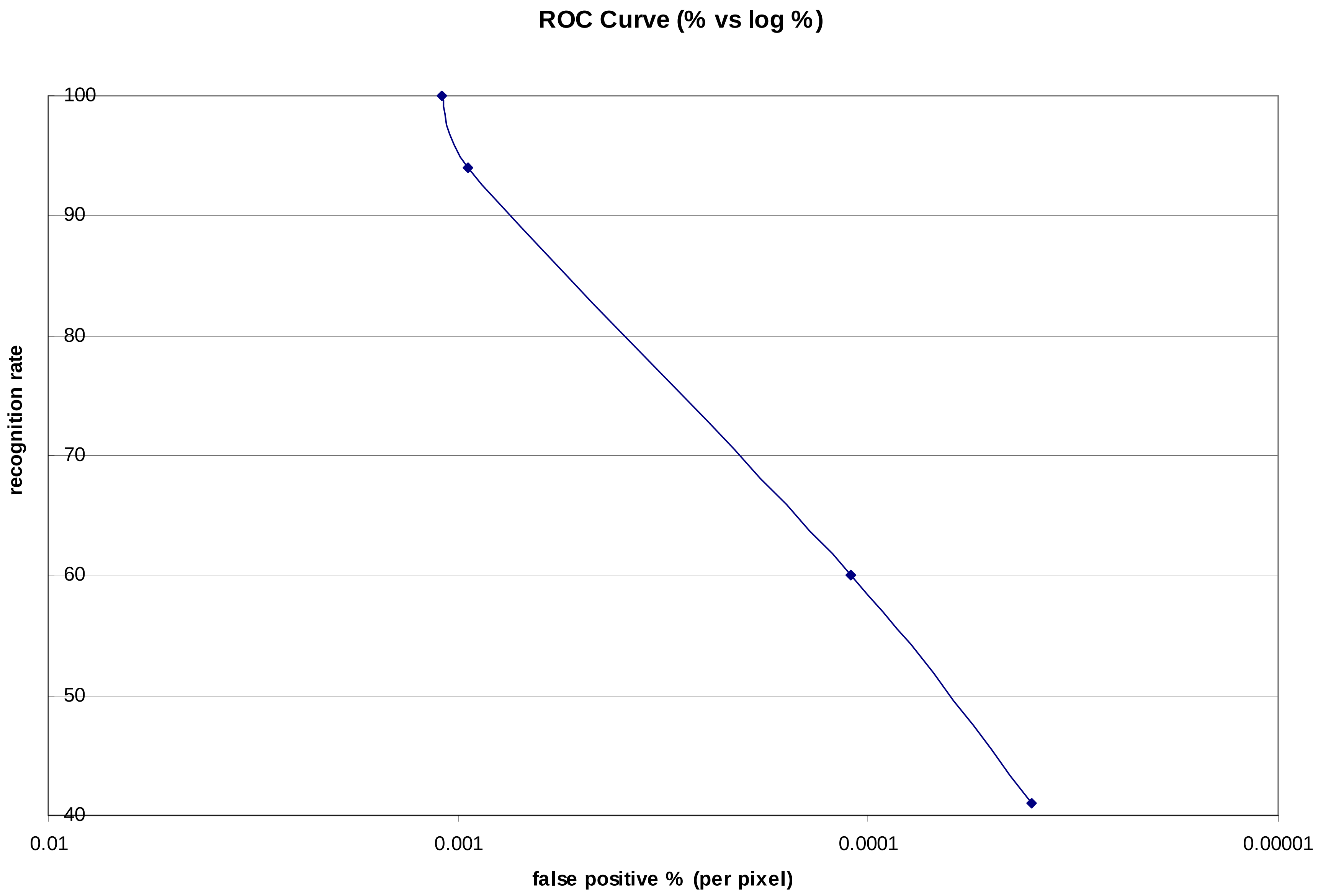
Target Sub-Window Outputs

Segmenting and Classification

Each sub-window is assigned to 1 of n groups based on it's nearness to prototypes derived from background & target data



Results



ROC Curve (% vs log %)
recognition rate
100
90
80
70
60
50
40
0.01
0.001
0.0001
0.00001
false positive % (per pixel)

Conclusion

- Current breadboard 3DANN processor demonstrates feasibility of a low power/mass high bandwidth analog processor for evaluating sensor data
- Can accommodate a wide range of sensor data processing problems as inner product/filtering is often a bottleneck for sensor processing algorithms
- Proceeding to develop next generation 3DANN with completely digital interface and a pre/post processing capability